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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/390,090	09/03/1999	ALAIN P. LEVESQUE	07923/120001	6316

7590 12/31/2002

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EXAMINER
ROUVAS, NIKOLAOS

ART UNIT	PAPER NUMBER
2614	

DATE MAILED: 12/31/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/390,090	LEVESQUE ET AL.	
	Examiner	Art Unit	
	Nikolaos Rouvas	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 13-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 13-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-11 and 13-24 have been considered but are moot in view of the new ground(s) of rejection.

In regards to claims 1 and 23, Yifrach discloses a "JB/F button" (column 3, line 41), which controls a logic circuit (as can also be seen in Figure 1). When this button is depressed, the logic circuit sends an appropriate signal to select a real-time or a time-shifted mode of operation (which, due to the nature of the opening and closing a circuit, i.e., on/off, is digital per say). In such a case, the Yifrach reference satisfies the claim limitations given the broadest reasonable interpretation thereof.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S Patent No. 5,329,320 to Yifrach.

In regards to claims 1 and 2, Yifrach discloses a buffer system for a television receiver, which provides the user with a "Normal-Viewing Mode" (column 1, lines 40-41) which displays the input signal in real time, and a "Delayed-Viewing Mode" (column 1, line 61) which produces a time-shifted output in relation to the real-time signal . A "Freeze Mode" (column 2, lines 3-4)

is also provided in one of the embodiments, where the user can choose to "freeze a portion of the broadcast" (column 4, line 35) and play it back in a delayed fashion via the "Freeze Button" and the "Playback Button" (column 4, lines 46-47). Yifrach discloses a "JB/F button" (column 3, line 41), which controls a logic circuit (as can also be seen in Figure 1). When this button is depressed, the logic circuit sends an appropriate signal to select a real-time or a time-shifted mode of operation (which, due to the nature of the opening and closing a circuit, i.e., on/off, is digital per say).

In regards to claim 3, Yifrach discloses an embodiment with a "Fast Forward button" and a "Return button" (column 5, lines 61-62) to allow the user to fast forward or rewind to a specific portion of the received signal when he's watching it in a delayed mode.

In regards to claim 4, the reference discloses a "JB/F" button (column 3, line 29), which is used to select the viewer's desired mode of operation (real-time or delayed).

In regards to claim 5, the reference discloses an antenna used "for receiving RF signals" (column 2, lines 59-60), which then get processed by the buffer system.

In regards to claim 23, Yifrach discloses a receiver and buffer system configured to provide the user with a real-time signal (corresponding to claimed "first signal") and a time-shifted signal (corresponding to claimed "second signal"). The claimed "encoder", "buffer", and "controller" are met by the corresponding elements of Figure 1, namely: 21, 23, and 26.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 6-10, 13-22, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S Patent No. 5,329,320 to Yifrach.

In regards to claim 6, the examiner takes OFFICIAL NOTICE that it's notoriously well-known in the art to buffer signals input to a television receiver in order to carry out video signal processing to condition the signals for display, i.e., to compensate for signal degradation as a result of transmission, to compensate for artifacts that arise as a result of the standard used, etc. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use an input frame buffer for the reasons indicated above.

In regards to claims 7, 8, and 10, Yifrach does not disclose input compressed video, a decoder to decompress the input compressed video signal, or MPEG video. However, the examiner submits that it would have been clearly obvious to one having ordinary skill in the art at the time the invention was made to modify Yifrach's receiver with the ability to receive and decode such signals so that it can operate in conjunction with a digital video distribution network employing the MPEG compression standard.

In regards to claim 9, the reference does not disclose a single codec chip that provides both operating modes. However, it would have been obvious to one having ordinary skill in the

art at the time the invention was made to use a single codec chip in order to reduce manufacturing costs, improve efficiency, and utilize space (on the circuit board).

In regards to claim 20, the reference does not disclose a real-time decoder or a frame storage system. The logic circuit of Figure 1, element 26, corresponds to the claimed "controller", and element 25, the D/A converter, corresponds to the claimed "time-shifted decoder" of amended claim 20. The system generates the appropriate output (time-shifted or real-time) according to the command it receives from the logic circuit, which is viewable by a display device such as the one in Figure 1, element 15. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a real-time decoder so that the system could operate in conjunction with a digital video distribution network. Modifying Yifrach's system so it would operate in a digital broadcast environment would also enable it to operate in response to a "digital video input signal" as cited in amended claim 20. It would have been obvious to one having ordinary skill in the digital television art at the time the invention was made to implement Yifrach's system in a digital broadcast environment to allow for better signal reception and compression capabilities. It would have been further obvious to one having ordinary skill in the art at the time the invention was made to use a frame storage system that would store digital video signals separately from the real-time decoder in order to use it as a means for retrieving desirable frames at a later time, while making efficient use of the storage capacity.

In regards to claim 21, the reference does not disclose a frame buffer or a frame storage system. However, as explained previously, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use frame buffers in order to compensate for

signal degradation as a result of transmission and to use a frame storage system as a means for retrieving desirable frames at a later time.

In regards to claim 22, the same reasons for rejecting claims 20 and 21 apply. The examiner submits that it would have been obvious to one having ordinary skill in the digital television art at the time the invention was made to implement Yifrach's system in a digital broadcast environment to allow for better signal reception and compression capabilities. With such a modification, Yifrach's system would be able to operate in response to a "digital video input" as cited in amended claim 22.

In regards to claims 13,14, and 16, see previous discussion about modifying Yifrach's receiver so that it can receive and decode compressed input signals. Referring to Figure 1, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Yifrach's receiver by inserting a decoder (the real-time one in this case) between elements 12 and 21 (so the path 11-12-21-22-23-24-25-13-15 would include two decoders) so that it could operate in conjunction with a digital video distribution network. It would have been further obvious to one having ordinary skill in the art at the time the invention was made to combine the two decoders or the encoder and decoder in a single codec chip in order to reduce manufacturing costs, improve efficiency, and utilize space (on the circuit board).

In regards to claim 15, Figure 1 discloses two paths: A real-time path as outlined by elements 11-12-13-15, and a delayed path as outlined by elements 11-12-21-22-23-24-25-13-15. Control circuitry that selects the mode of transmission is represented by elements 26 and 27, and further described in column 3, lines 28-32. Finally, the processing paths include an encoder (element 22) and a decoder (element 24).

In regards to claim 17, see previous discussion regarding claim 6, where buffers are commonly used in television receivers to compensate for signal degradation. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a common memory for the buffers in order to minimize cost, and utilize buffer space.

In regards to claim 18, Yifrach discloses his system as being part of a television receiver. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement Yifrach's teachings in a set-top box in order to be able to provide service to viewers in a video distribution system that uses set-top boxes.

In regards to claim 19, Yifrach discloses an analog picture tube or screen in Figure 1, element 15.

In regards to claim 24, Yifrach is silent on whether the transition from the real-time mode to the time-shifted mode is seamless. However, in receiver/buffer systems such as the one Yifrach discloses, buffers are used in order to minimize delays. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to make the transition seamless in order to provide a more appealing video presentation to the user.

2. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yifrach in further view of U.S. Patent No. 5,701,383 to Russo et al.

In regards to claim 11, Yifrach does not disclose any means for identifying the paused frame, but Russo et. al discloses means for storing information relating to a specific point in a program when a "PAUSE command" (column 3, lines 10-11) is received, or, in another embodiment, when a "MARK command" (column 3, line 48) is issued and used along with "Marker memory" (column 8, line 20) where information regarding program markers is stored,

to specify a point from which playback can be resumed. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use such means as the ones explained above for purposes of indexing frames.

Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Nikolaos Rouvas** whose telephone number is **(703) 305-6955**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **John Miller**, can be reached at **(703) 305-4795.**

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

JOHN MILLER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600